130512 / 4AA064 / 6-15

HPR 400 Transceiver Unit

This document describes the design, theory of operation, and part replacement procedures, of the HPR 400 Transceiver Unit. The unit is used in all the HPR 400 series Hydroacoustic Position Reference (HPR) systems supplied by Kongsberg Simrad AS.

Document revisions

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A	14.06.94	NB	HPJ	JEF
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D				
E				
F				
G				

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Contents

Document history

(The information on this page is for internal use)

Rev. A Original edition based on P2421, document "C", rev. A.

Rev. B Document updated, some unnecessary information removed, some block diagrams added. Document reformatted to Ileaf 6.1.

Rev. C DSPM and CPU pcbs changed. Other minor corrections. Ref. 130512C.

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1 INTRODUCTION

This technical description is created to assist the maintenance engineer with intermediate level maintenance operations. This means that the maintenance technician or engineer is expected to replace faulty Line Replaceable Units (LRU) (circuit boards or modules), but not to perform circuit board repairs. In order to find the faulty component, it is further expected that the maintenance personnel have access to standard electronic instruments, such as oscilloscopes and multimeters.

The personnel designated to perform maintenance on this unit (and the rest of the system) should be well qualified technical personnel, with experience of computer–based electronic circuitry. It is also strongly recommended that the personnel are familiar with the basic principles of hydroacoustic technology, and in particular, positioning systems.

Training courses are available from Kongsberg Simrad AS.

2 GENERAL INFORMATION

2.1 Design

The Transceiver Unit is constructed of aluminium panels and extruded strip. One of several different cover panel designs may be used depending on the type of installation (console, desk–top, rack, or portable). The dismantling procedures described in this manual refer to the unit as used in the console or 19" rack.

The majority of the circuit boards contained in the unit are standard single–Europa cards, accessible by opening the front of the unit. The cards are plug–in units, held in position by plastic clips.

3 mm Ø holes are drilled in the upper and lower front corners of each board. These are to attach the wire handle used to extract the board from the unit.

2.2 Maintenance actions

The corrective maintenance on the Transceiver Unit is limited to operational checks and circuit board replacements. An extension board will be required if the maintenance engineer wishes to perform measurements on the boards during system operation. This is delivered with the standard spare parts kit for the Transceiver Unit.

2.3 External connections

All external connections to the Transceiver Unit are made via plugs located on the rear of the unit. Refer to chapter NO TAG for further information.

2.4 Power supply

The Transceiver Unit can be powered from either a 115 Vac or 230 Vac supply. Links must be set inside the unit to adapt the unit to the voltage supply. A mains power switch is located on the front panel, together with a *Power on* indicator lamp.

3 THEORY OF OPERATION

3.1 Introduction

The HPR 400 Transceiver Unit is the central part of the HPR system. It contains the following:

- Electronic circuitry for transmission of acoustic pulses
- Amplifiers and filters for reception of acoustic signals
- Interfaces to external sensors
- Serial line for communication with the Beam Control Unit (for tracking systems)
- Serial line for communication with the System Controller (an Ethernet link will be available shortly).

The Transceiver Unit's main navigation function is to interrogate transponders and measure the range and bearing to them. The main telemetry function is to transmit and receive acoustic signals.

3.2 Navigation

The operator selects the active mode of operation. The system can then switch automatically between the selected mode and the other available mode(s). This means that the system can make use of several different types of transponder in the same operation.

3.3 SSBL

In this mode, both direction and range to the transponder(s) are computed.

When a transponder is switched on by the operator, the transceiver will start interrogation using frequencies corresponding to the applicable transponder channel. This is achieved by controlling the transmitter and receiver (preamplifier) boards. The Central Processing Unit (CPUEX) circuit board measures the time elapsed from the interrogation (transmission) till the pulse is detected by the Digital Signal Processor (DSPM) board.

The three "R", "X" and "Y" signals received from the HPR transducer will first enter the Input A or Input B preamplifier circuit boards where they are amplified and filtered. The signals are then sampled and converted to binary format by the Analogue/Digital Converter (ADCM) circuit board. The DSPM 50 reads the data on the ADCM output, detects the signals, and calculates the phase differences between the "R" and "X" input channels and the "R" and "Y" input channels.

The DSPM 50 transfers the received data to the CPUEX circuit board, which then calculates the "X", "Y" and "R" coordinates to the transponder. In this calculation, the data from the external vertical reference unit and compass is used to compensate for the roll and pitch of the vessel. The sensor data is received and converted by the Input Output (IOM) circuit board. When the positioning calculations has been terminated, the current position is sent to the System Controller, and a new interrogation sequence can begin.

3.4 LBL positioning

In this mode, only the ranges to the transponders are computed, and several ranges are then used to triangulate the position.

The functional operation is basically the same as for SSBL. However, in the LBL mode the transceiver will await replies from all the transponders in the transponder array before it starts on a new interrogation sequence. The system uses the R channel to detect the range.

3.5 SSBL and LBL

In this mode, both range and direction to the transponder(s) are computed.

This mode is a combination of the SSBL and LBL modes described above, and the functional operation is basically identical to the SSBL. However, the transceiver will await replies from all the transponders in the array before starting a new interrogation sequence.

3.6 Telemetry

The operator may select this mode when he/she wishes to send and receive telemetry messages, for example to read the battery status of a transponder. When the transceiver reads the telemetry message from the System Controller, it will convert the message into acoustic signals. This acoustic message contains bursts and pulses with different frequencies and fixed intervals. The transceiver transmits the message(s), and will await the telemetry reply.

The signal path is identical as for navigation mode. The DSPM 50 will calculate the frequency of the current reception, and report this to the CPUEX. The CPUEX will assemble the frequency data, and decode the message from acoustic pulses into digital values. The data is then passed on to the System Controller.

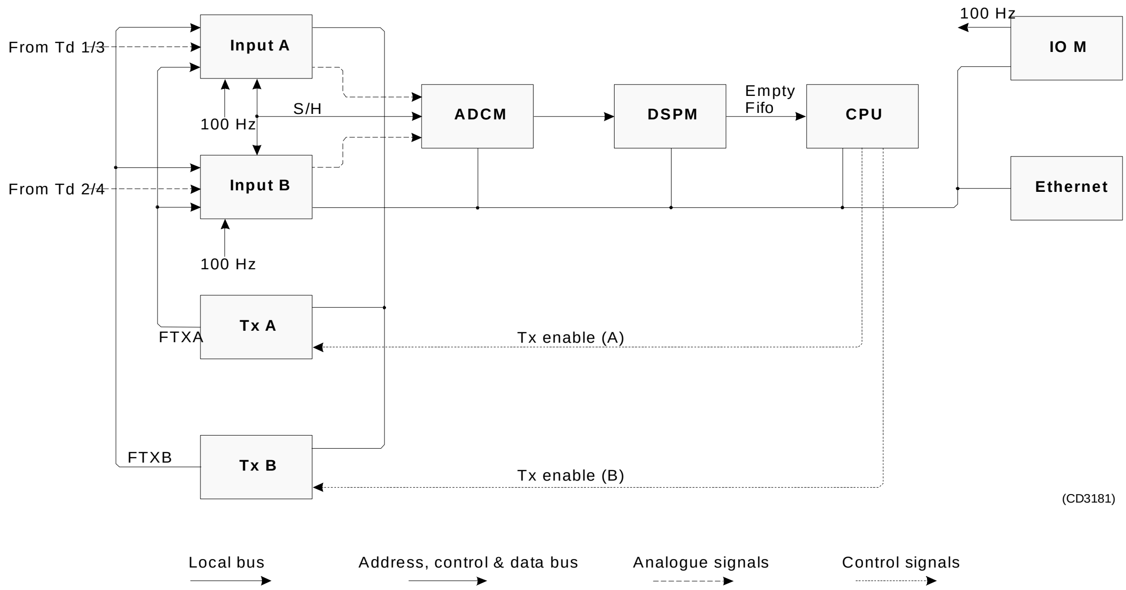

Figure 1 HPR 400 Transceiver unit – functional block diagram

3.7 Circuit board identification and main functions

- **Central Processing Unit (CPUEX)**
  - Position calculation
  - Loads and controls the DSPM 50 program
  - Serial line to CDU
  - Controls Tx/Rx hardware
- **Digital Signal Processor (DSPM 50)**
  - Reads data from ADCM
  - Performs pulse detection
  - Performs digital filtering (Fast Fourier Transformations)
- **Analog Digital Converter (ADCM)**
  - Samples the data from INPUTM
  - Converts to binary format
- **Input (INPUTM)**
  - 8–channel receiver
  - Amplifies
  - Bandpass filtering
  - Sample/hold circuitry
- **Transmitter (TXM)**
  - Transmitter
  - Frequency generator for Rx and Tx frequency

- **Input & Output (IOM)**
  - Interface to vertical reference unit (analogue)
  - Interface to gyro (synchro and serial line)
  - TVG initialization
  - Clock for phase locked loop on INPUTM
- **Ethernet (ENET–M)**
  - Ethernet interface
- **Motherboard**
  - Connects all the individual circuit boards together

4 CONNECTIONS

All connections to and from the HPR 400 Transceiver Unit are made on the connection panel on the rear of the unit. All connectors are male except where stated female.

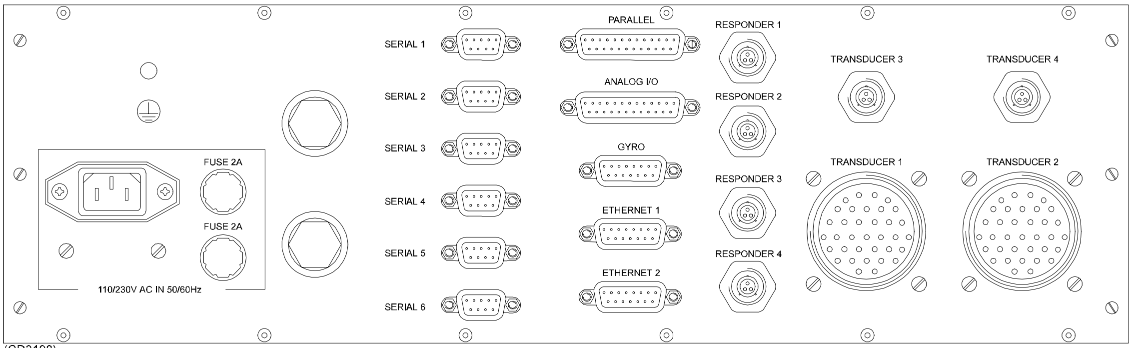

Figure 2 The connectors on the Transceiver Unit's rear panel

This panel holds the following connectors and fuses (top to bottom, left to right when looking at the rear panel):

1 Standard 3–pin, 230 Vac, 50/60 Hz mains power in.

2 Fuse, 230 Vac, 2 A.

3 Fuse, 230 Vac, 2 A.

4 9–pin D–connector for Serial line 1.

5 9–pin D–connector for Serial line 2.

6 9–pin D–connector for Serial line 3.

7 9–pin D–connector for Serial line 4.

8 9–pin D–connector for Serial line 5.

9 9–pin D–connector for Serial line 6.

10 25–pin D–connector for Parallel input.

11 25–pin D–connector for Analogue input/output.

12 15–pin D–connector for Gyro input.

13 15–pin D–connector for Ethernet 1.

14 15–pin D connector for Ethernet 2.

15 3–pin Amphenol connector for Responder 1.

16 3–pin Amphenol connector for Responder 2.

17 3–pin Amphenol connector for Responder 3.

18 3–pin Amphenol connector for Responder 4.

19 3–pin Amphenol connector for Transducer 3.

20 3–pin Amphenol connector for Transducer 4.

21 35–pin Amphenol connector for Transducer 1.

22 35–pin Amphenol connector for Transducer 2.

Note ! *The two white plastic caps are the securing nuts for two capacitors located on the inside of the Transceiver Unit rear panel.*

All connectors are marked with labels as indicated on the previous drawing.

5 INTERNAL LAYOUT

The Transceiver Unit holds the following circuit boards and power units:

From left to right:

- Input M – A/B.
- A/D Converter (ADCM).
- Digital Signal Processor (DSPM 50).
- Control Processing Unit (CPUEX).
- Ethernet.
- Spare.
- Input/Output (IOM).
- Responder (RPC) (Option).
- Transmitter (TXM – A/B).
- DC Power supply (DC – PWR).
- AC Power supply (AC – PWR).

The backplane is located behind the circuit boards, and is accessible through the rear of the Transceiver Unit. All the circuit boards and power units must be removed through the front of the unit before the backplane can be removed. All connections to the backplane are made using plugs.

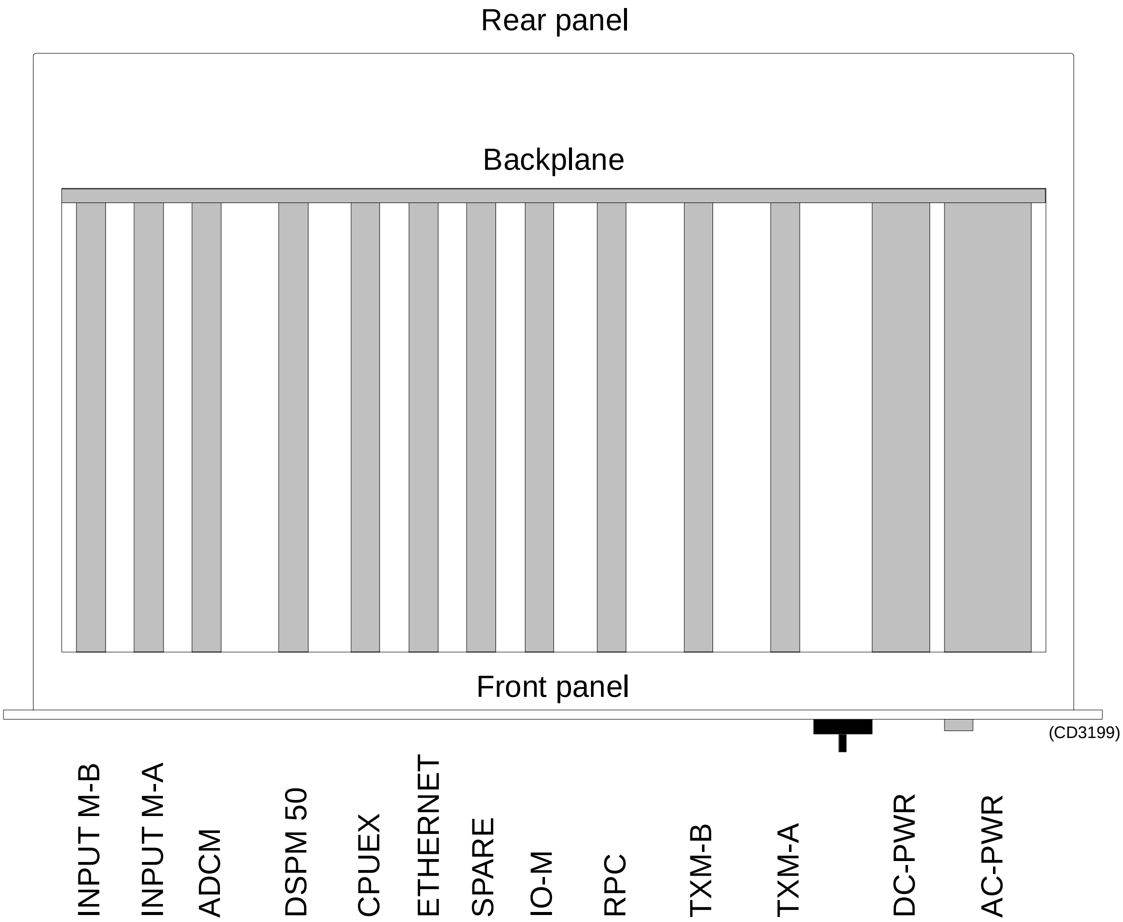

Figure 3 HPR 400 Transceiver Unit – internal layout

6 CIRCUIT BOARD DESCRIPTIONS

6.1 General

This section provides a full functional description of each of the circuit boards contained within the HPR 400 Transceiver Unit. Refer to chapter 3 for a description of the Transceiver Unit's theory of operation.

6.2 The backplane

6.2.1 Board description

The backplane is located in the back of the Transceiver Unit. It is the interconnection circuit board, carrying connectors and wiring tracks to interconnect the other circuit boards in the Transceiver Unit. All the other circuit boards plug into the backplane.

6.2.2 Main components

The board holds the following three ICs:

- U01 . . 74HC240 Buffer, inverted on outputs
- U02 . . PAL 20V8 Address decoder. (For TX–PCBs only)
- U03 . . . . 74HC123F Retriggerable monostable multivibrator

6.2.3 Socket mounted components

The board holds only one socket–mounted component:

- U02PAL 20V8 Address decoder. (For TX–PCBs only)

6.2.4 Connections

There are 37 connectors on the circuit board, mounted on both sides. Connectors J1 to J12 are 96–pin Europa connectors for the single Euro–card circuit boards in the unit. For the pin configurations, refer to the following drawing:

HPR 400 Backplane 824–108544 (SH–067)

J1 . . . . Input–B

J2 . . . . Input–A

J3 . . . . ADCM

J4 . . . . DSPM

J5 . . . . CPU

J6 . . . . Ethernet

J7 . . . . Spare

J8 . . . . IO–M

J9 . . . . RPC

J10 . . . . TXM–B

J11 . . . . TXM–A

J12 . . . . POWERM

P14 . . . . 8–pin Phoenix plug, male

P15 . . . . 50–pin 3M, male, flat ribbon cable connector
P16 . . . . 18–pin Molex, male
P17 . . . . 8–pin Phoenix plug, male
P18 . . . . 2–pin Phoenix plug, male
P19 . . . . 2–pin Phoenix plug, male
P20 . . . . 2–pin Phoenix plug, male
P21 . . . . 34–pin 3M, male, flat ribbon cable connector
P22 . . . . 50–pin 3M, male, flat ribbon cable connector
P23 . . . . 50–pin 3M, male, flat ribbon cable connector
P24 . . . . 2–pin Phoenix plug, male
P25 . . . . 2–pin Phoenix plug, male
P26 . . . . 9–pin Molex, male
P27 . . . . 3–pin Molex, male
P28 . . . . 9–pin Molex, male
P29 . . . . 3–pin Molex, male
P30 . . . . 6–pin Molex, male
P31 . . . . 9–pin Molex, male
P32 . . . . 3–pin Molex, male
P33 . . . . 9–pin Molex, male
P34 . . . . 3–pin Molex, male
P35 . . . . 6–pin Molex, male
P36 . . . . 3–pin Molex, male
P37 . . . . 3–pin Molex, male
P38 . . . . 3–pin Molex, male

6.2.5 Pin assignments

P14 pin assignments		
Pin	**Signal**	**Description**
1	TD 2, Tx+	Transducer 2, transmission +
2	TD 2, Tx–	Transducer 2, transmission –
3	TD 4, Tx+	Transducer 4, transmission +
4	TD 4, Tx–	Transducer 4, transmission +
5	+15 Vdc	
6	–15 Vdc	
7	AGND	Analogue ground
8	DGND	Digital ground

P15 pin assignments			
Pin	**Signal**	**Description**	**Ext.**
1	RS422_Rx1	RS422+ serial line. To CPU .... Input	1
2	RS422_Tx1–	RS422– serial line. From CPU .... Output	6
3	RS232_Rx	RS232 serial line. To CPU .... Input	2
4			7
5	RS232_Tx	RS232 serial line. From CPU .... Output	3
6			8
7	RS422_Rx1–	RS422– serial line. To CPU .... Input	4
8	RS422_Tx1	RS422+ serial line. From CPU .... Output	9
9	GND1	Galvanically isolated ground	5
10	RS422_Rx2	RS422+ serial line 2 .... Input	1
11	RS422_Tx2–	RS422– serial line 2 .... Output	6
12			2
13			7
14			3
15			8
16	RS422_Rx2–	RS422– serial line 2 .... Input	4
17	RS422_Tx2	RS422+ serial line 2 .... Output	9
18	GND	Ground	5
19	RS422_Rx3	RS422+ serial line 3 .... Input	1
20	RS422_Tx3–	RS422– serial line 3 .... Output	6
21			2
22			7
23			3
24			8
25	RS422_Rx3–	RS422– serial line 3 .... Input	4
26	RS422_Tx3	RS422+ serial line 3 .... Output	9
27	GND	Ground	5
28	SY1_in	External sync1+ .... Input	1
29	SY1_out–	External sync1– .... Output	6
30	SY2_out–	External sync2– .... Output	2
31	SY2_in	External sync2+ .... Input	7
32	SY2_out	External sync2+ .... Output	3
33	SY2_in–	External sync2– .... Input	8
34	SY1_in–	External sync1– .... Input	4
35	SY1_out	External sync1+ .... Output	9
36	GND	Ground	5

P15 pin assignments			
Pin	**Signal**	**Description**	**Ext.**
37	ANA_1	Analogue 1 . . . . Input	14
38	AGND	Analogue ground	2
39	ANA_2	Analogue 2 . . . . Input	15
40	AGND	Analogue ground	3
41			16
42			4
43			17
44			5
45	S1	Synchro gyro S1 . . . . Input	1
46	R.Hi	Reference high R.Hi . . . . Input	9
47	S2	Synchro gyro S2 . . . . Input	2
48	R.L	Reference low R.L . . . . Input	10
49	S3	Synchro gyro S3 . . . . Input	3
50			11

Abbreviations: SY = Synch, ANA = Analogue

P16 pin assignment	
Pin	**Description**
1	+24 volt, responder 1
2	Trigger, responder 1
3	Digital ground
4	Analogue ground
5	+24 volt, responder 2
6	Trigger, responder 2
7	Digital ground
8	Analogue ground
9	+24 volt, responder 3
10	Trigger, responder 3
11	Digital ground
12	Analogue ground
13	+24 volt, responder 4
14	Trigger, responder 4
15	Digital ground
16	Analogue ground
17	–
18	–

P17 pin assignment		
Pin	**Signal**	**Description**
1	TD 1, Tx+	Transducer 1, transmission +
2	TD 1, Tx–	Transducer 1, transmission –
3	TD 3, Tx+	Transducer 3, transmission +
4	TD 3, Tx–	Transducer 3, transmission +
5	+15 Vdc	
6	–15 Vdc	
7	AGND	Analogue ground
8	DGND	Digital ground

P18 pin assignment		
Pin	**Signal**	**Description**
1	TxA CAP + ...	Capacitor A . . . . +48 Vdc
2	TxA CAP –	Capacitor A . . . . 0 V

P19 pin assignment		
Pin	**Signal**	**Description**
1	TxB CAP + ...	Capacitor B . . . . +48 Vdc
2	TxB CAP –	Capacitor B . . . . 0 V

P20 pin assignment	
Pin	**Description**
1	+48 Vdc from AC power supply
2	Analogue ground

P21 pin assignments			
Pin	**Signal**	**Description**	**Ext.**
1	RXAI	RS422+ serial line A .... Input	1
2	TXA/	RS422– serial line A .... Output	6
3	RXA	RS232 serial line A .... Input	2
4	RXCB	RX clock TTL .... Input	7
5	TXA	RS232 serial line A .... Output	3
6	CTSA/	Clear to send A TTL .... Input	8
7	RXA/	RS422– serial line A .... Input	4
8	TXA0	RS422+ serial line A .... Output	9
9	GND	Ground reference A	5
10	RXBI	RS422+ serial line B .... Input	1
11	TXB/	RS422– serial line B .... Output	6
12	RXB	RS232 serial line B .... Input	2
13	TXCB	RX clock TTL .... Input	7
14	TXB	RS232 serial line B .... Output	3
15	CTSB/	Clear to send B TTL .... Input	8
16	RXB/	RS422– serial line B .... Input	4
17	TXB0	RS422+ serial line B .... Output	9
18	GND	Ground reference B	5
19	IO1	Digital input/output .... Input/Output	1
20	IO2	Digital input/output .... Input/Output	2
21	IO3	Digital input/output .... Input/Output	3
22	IO4	Digital input/output .... Input/Output	4
23	IO5	Digital input/output .... Input/Output	5
24	IO6	Digital input/output .... Input/Output	6
25	IO7	Digital input/output .... Input/Output	7
26	IO8	Digital input/output .... Input/Output	8
27	RXCB	RX clock TTL .... Input	9
28	TXCB	TX clock TTL .... Input	10
29	CTSB/	Clear to send B TTL .... Input	11
30	CTSA/	Clear to send A TTL .... Input	12
31	GND	Power ground	13
32	GND	Power ground	14
33	+5 Vdc	+5 Vdc power supply .... Output	15
34	+5 Vdc	+5 Vdc power supply .... Output	16

P22 pin assignments			
Pin	**Signal**	**Description**	**Ext.**
1	RS422_Rx1	RS422+ serial line. To CPU .... Input	1
2	RS422_Tx1–	RS422– serial line. From CPU .... Output	6
3	RS232_Rx	RS232 serial line. To CPU .... Input	2
4			7
5	RS232_Tx	RS232 serial line. From CPU .... Output	3
6			8
7	RS422_Rx1–	RS422– serial line. To CPU .... Input	4
8	RS422_Tx1	RS422+ serial line. From CPU .... Output	9
9	GND1	Galvanically isolated ground	5
10	RS422_Rx2	RS422+ serial line 2 .... Input	1
11	RS422_Tx2–	RS422– serial line 2 .... Output	6
12			2
13			7
14			3
15			8
16	RS422_Rx2–	RS422– serial line 2 .... Input	4
17	RS422_Tx2	RS422+ serial line 2 .... Output	9
18	GND	Ground	5
19	RS422_Rx3	RS422+ serial line 3 .... Input	1
20	RS422_Tx3–	RS422– serial line 3 .... Output	6
21			2
22			7
23			3
24			8
25	RS422_Rx3–	RS422– serial line 3 .... Input	4
26	RS422_Tx3	RS422+ serial line 3 .... Output	9
27	GND	Ground	5
28	SY1_in	External sync1+ .... Input	1
29	SY1_out–	External sync1– .... Output	6
30	SY2_out–	External sync2– .... Output	2
31	SY2_in	External sync2+ .... Input	7
32	SY2_out	External sync2+ .... Output	3
33	SY2_in–	External sync2– .... Input	8
34	SY1_in–	External sync1– .... Input	4
35	SY1_out	External sync1+ .... Output	9
36	GND	Ground	5

P22 pin assignments			
Pin	**Signal**	**Description**	**Ext.**
37	RXBI	RS422+ serial line B .... Input	1
38	TXB/	RS422– serial line B .... Output	6
39	RXB	RS232 serial line B .... Input	2
40	TXCB	RX clock TTL .... Input	7
41	TXB	RS232 serial line B .... Output	3
42	CTSB/	Clear to send B TTL .... Input	8
43	RXB/	RS422– serial line B .... Input	4
44	TXB0	RS422+ serial line B .... Output	9
45	GND	Ground reference B	5
46			
47			
48			
49			
50			

Pins 1 through 9 will connect to the external plug Serial I, on backplane (from IOM, P2 pins 1→9 P15 pins 1→9).

Pins 10 through 18 will connect to the external plug Serial II, on backplane (from IOM, P2 pins 10→18 P15 pins 10→18).

Pins 19 through 27 will connect to the external plug Serial III, on backplane (from IOM, P2 pins 19→27 P15 pins 19→27).

Pins 28 through 36 will connect to the external plug Serial IV, on backplane (from IOM, P2 pins 28→36 P15 pins 28→36).

Pins 37 through 45 will connect to the external plug Serial V, on backplane (from CPU, P2 pins 10→19 P21 pins 10→19).

Pins 46 through 50 will connect to the external plug Serial VI (Debug), on backplane (from CPU, P2).

P23 pin assignments			
Pin	**Description**	**Pin**	**Description**
1	IO5, Digital input/output	26	GND
2	IO6, Digital input/output	27	PC0 (Analogue 1)
3	IO7, Digital input/output	28	PC1 (Ground)
4	IO8, Digital input/output	29	PC2 (Analogue 2)
5	CLK 0	30	PC3 (Ground)
6	GATE 1	31	PC4 (Analogue 3)
7	T0 out	32	PC5 (Ground)
8	T1 out	33	PC6 (Analogue 4)
9	GND	34	PC7 (Ground)
10	PB7	35	GND

P23 pin assignments			
Pin	**Description**	**Pin**	**Description**
11	PB6	36	DIFF 1– (S1, synchro)
12	PB5	37	DIFF 1 (Rh, ref. high)
13	PB4	38	DIFF 2– (S2, synchro)
14	PB3	39	DIFF 2 (Rl, ref. low)
15	PB2	40	DIFF 3– (S3 synchro)
16	PB1	41	DIFF 3
17	PB0	42	GND
18	PA7	43	AN_IN 8 (VRU +15 V)
19	PA6	44	AN_IN 7 (Analogue ground)
20	PA5	45	AN_IN 6 (VRU –15 V)
21	PA4	46	AN_IN 5 (Roll)
22	PA3	47	AN_IN 4 (Common)
23	PA2	48	AN_IN 3 (Pitch)
24	PA1	49	AN_IN 2 (Analogue ground)
25	PA0	50	AN_IN 1

Signal descriptions for P23				
Signal	**From**	**Via**	**Via**	**To**
Analogue 1	IO/M P2 37	P15 pin 37	P23 pin 27	ANALOGUE I/O pin 14
GND	IO/M P2 38	P15 pin 38	P23 pin 28	ANALOGUE I/O pin 2
Analogue 2	IO/M P2 39	P15 pin 39	P23 pin 29	ANALOGUE I/O pin 15
GND	IO/M P2 40	P15 pin 40	P23 pin30	ANALOGUE I/O pin 3
S1	IO/M P2 45	P15 pin 45	P23 pin36	GYRO pin 1
Rh	IO/M P2 46	P15 pin 46	P23 pin37	GYRO pin 9
S1	IO/M P2 47	P15 pin 47	P23 pin38	GYRO pin 2
R1	IO/M P2 48	P15 pin 48	P23 pin39	GYRO pin 10
S3	IO/M P2 49	P15 pin 49	P23 pin40	GYRO pin 3
VRU +15 Vdc	IO/M P1 c23	P23 pin 43		ANALOGUE I/O pin 22
GND	IO/M P1 b2	P23 pin 44		ANALOGUE I/O pin 10
VRU –15 Vdc	IO/M P1 a2	P23 pin 45		ANALOGUE I/O pin 23
Roll	IO/M P1 c22	P23 pin 46		ANALOGUE I/O pin 11
Common	IO/M P1 b2	P23 pin 47		ANALOGUE I/O pin 24
Pitch	IO/M P1 a2	P23 pin 48		ANALOGUE I/O pin 12
Analogue ground	IO/M P1 c21	P23 pin 49		ANALOGUE I/O pin 25

P24 pin assignment (DC input)	
Pin	**Description**
1	+48 Vdc backup
2	Analogue ground

P25 pin assignment (External responder power)		
Pin	**Signal**	**Description**
1	Ext. pwr RSP	Responder power
2	AGND	Analogue ground

P26 pin assignment (To Input–A pcb, channels 1 – 3)		
Pin	**Signal**	**Description**
1	A INA_1	Input A, channel 1 IN +
2	A INBA_1	Input A, channel 1 IN –
3	AGND	Analogue ground
4	A INA_2	Input A, channel 2 IN +
5	A INB_2	Input A, channel 2 IN –
6	AGND	Analogue ground
7	A INA_3	Input A, channel 3 IN +
8	A INB_3	Input A, channel 3 IN –
9	AGND	Analogue ground

P27 pin assignment (To Input–A pcb, channel 4)		
Pin	**Signal**	**Description**
1	A INA_4	Input A, channel 4 IN +
2	A INB_4	Input A, channel 4 IN –
3	AGND	Analogue ground

P28 pin assignment (To Input–A pcb, channels 5 – 7)		
Pin	**Signal**	**Description**
1	A INA_5	Input A, channel 5 IN +
2	A INB_5	Input A, channel 5 IN –
3	AGND	Analogue ground
4	A INA_6	Input A, channel 6 IN +
5	A INB_6	Input A, channel 6 IN –
6	AGND	Analogue ground
7	A INA_7	Input A, channel 7 IN +
8	A INB_7	Input A, channel 7 IN –
9	AGND	Analogue ground

P29 pin assignment (To Input–A pcb, channel 8)		
Pin	**Signal**	**Description**
1	A INA_8	Input A, channel 8 IN +
2	A INB_8	Input A, channel 8 IN –
3	AGND	Analogue ground

P30 pin assignment (For transducer 1)		
Pin	**Signal**	**Description**
1	ST 24, VC_B	Voltage control B, Td 1
2	DGND	Digital ground
3	AGND	Analogue ground
4	N/W–signal	Narrow/Wide Td 1
5	AGND	Analogue ground
6	Screen	

P31 pin assignment (To Input–B pcb, channels 1 – 3)		
Pin	**Signal**	**Description**
1	B INA_1	Input B, channel 1 IN +
2	B INBA_1	Input B, channel 1 IN –
3	AGND	Analogue ground
4	B INA_2	Input B, channel 2 IN +
5	B INB_2	Input B, channel 2 IN –
6	AGND	Analogue ground
7	B INA_3	Input B, channel 3 IN +
8	B INB_3	Input B, channel 3 IN –
9	AGND	Analogue ground

P32 pin assignment (To Input–B pcb, channel 4)		
Pin	**Signal**	**Description**
1	B INA_4	Input B, channel 4 IN +
2	B INB_4	Input B, channel 4 IN –
3	AGND	Analogue ground

P33 pin assignment (To Input–B pcb, channels 5 – 7)		
Pin	**Signal**	**Description**
1	B INA_5	Input B, channel 5 IN +
2	B INB_5	Input B, channel 5 IN –
3	AGND	Analogue ground
4	B INA_6	Input B, channel 6 IN +
5	B INB_6	Input B, channel 6 IN –
6	AGND	Analogue ground
7	B INA_7	Input B, channel 7 IN +
8	B INB_7	Input B, channel 7 IN –
9	AGND	Analogue ground

P34 pin assignment (To Input–A pcb, channel 8)		
Pin	**Signal**	**Description**
1	B INA_8	Input B, channel 8 IN +
2	B INB_8	Input B, channel 8 IN –
3	AGND	Analogue ground

P35 pin assignment (For transducer 2)		
Pin	**Signal**	**Description**
1	ST 25, VC_D	Voltage control D, Td 2
2	DGND	Digital ground
3	AGND	Analogue ground
4	N/W–signal	Narrow/Wide Td 2
5	AGND	Analogue ground
6	Screen	

P36 pin assignment (For transducer 3) Note ! External cable from P36 to Input–A pcb, channel 8		
Pin	**Signal**	**Description**
1	ALNK_A1	Telemetry (+) TxMB to input A
2	ALNK_A2	Telemetry (–) TxMB to input A
3	AGND	Analogue ground

P37 pin assignment (For transducer 4) Note ! External cable from P36 to Input-B pcb, channel 8		
Pin	**Signal**	**Description**
1	ALNK_B1	Telemetry (+) TxMB to input B
2	ALNK_B2	Telemetry (–) TxMB to input B
3	AGND	Analogue ground

P38 pin assignment		
Pin	**Signal**	**Description**
1	“ON”, (diode)	Power ON
2	GND	Ground
3	“CPU” (diode)	Not connected

6.2.6 Maintenance aids

6.2.6.1 Links

LK 1 . . . . 0 V for responder power. Link **IN** means internal power

LK 2 . . . . +48 V for responder power. Link **IN** means internal power

ST 1 . . . . Link 1–2 for VC_B to Input–A P1 c7

ST 1 . . . . Link 2–3 for VC_A to Input–A P1 c7 (Normally closed)

Seen from rear: **._.** .

ST 2 . . . . Link 1–2 for VC_D to Input–B P1 c7

ST 2 . . . . Link 2–3 for VC_C to Input–B P1 c7 (Normally closed)

Seen from rear: **._.** .

ST 7 . . . . EXRDY– Normally out

ST24 . . . . VC_B, (TVG), TD1. Normally in

ST25 . . . . VC_D, (TVG), TD2. Normally in

ST26 . . . . Link 1–2 for VEE(–5 V) to Input A/B P1 abc 28

ST26 . . . . Link 2–3 for VCC(+5 V) to Input–A/B P1 abc 28 (Normally closed)

Seen from rear: . **._.**

6.3 Input–M

6.3.1 Location and purpose

The HPR 400 Transceiver Unit holds two Input–M boards, B and A . These are located in the rack in the first and second slots from the left respectively. The purpose of the Input–M circuit board is to amplify transducer signals, perform demodulation and narrow band filtering, and present the output signals via Sample and hold circuitry.

6.3.2 Physical description

The Input–M board is a single Euro–card circuit board.

6.3.3 Circuit description

The Input–M circuit board is designed for eight individual channels, using identical analogue channel hybrid circuits. However, only five are fitted. The first four (grouped) are used for the SSBL system, the fifth (set apart from the others) is for the LBL system. The board is also equipped with digital circuitry common to all the analogue channels.

The circuit board's eight inputs from the transducer(s) are balanced, and individual input transformers are implemented. Each channel has a broad–band amplifier with voltage–controlled gain. The maximum gain is 75 dB relative to 1 V. If the transducer has its own internal amplifier, the signals may be routed directly to the filters by hardware straps.

The demodulators operate either with a common modulator frequency, with a common frequency for each of the two groups, or with an external frequency. The frequency is generated on the Input–M board, but it is controlled by the Central Processing Unit (CPU) board.

The low pass filters operate with a pass–band. The filters are controlled by a clock on the board, which in turn is controlled by the CPU. All the filters operate with the same bandwidth.

The outputs from each channel are the sine and cosine (real and imaginary) vectors of the demodulated signals. The analogue range is 0 to ± 2.5 Vdc. All the outputs are sampled by an external sample signal, and the values are stored until the next sample command arrives.

There are two frequency generators for the demodulators. They operate at 4 times the signal frequency, in steps of 100 Hz.

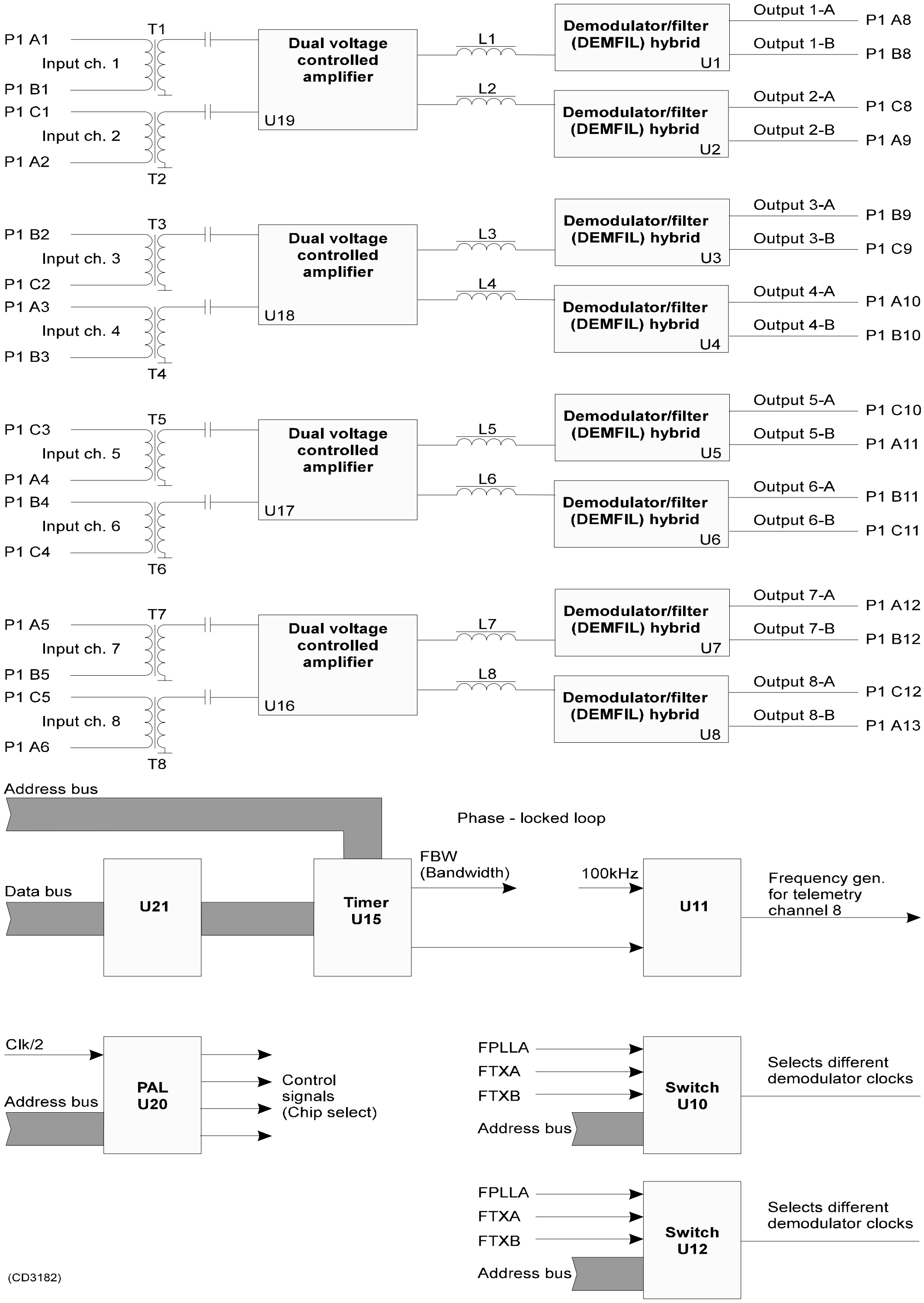

Figure 4 The Input M A/B circuit board – block diagram

6.3.4 Connections

The Input–M board carries one connector. This is a 96–pin Europa connector mounted on the rear edge of the board, used to link the board into the backplane.

P1 pin assignment 96–pin Europa connector			
Pin	**A**	**B**	**C**
1	IN1–A	IN1–B	IN2–A
2	IN2–B	IN3–A	IN3–B
3	IN4–A	IN4–B	IN5–A
4	IN5–B	IN6–A	IN6–B
5	IN7–A	IN7–B	IN8–A
6	IN8–B		
7	VCA		VCB
8	OUT1–A	OUT1–B	OUT2–A
9	OUT2–B	OUT3–A	OUT3–B
10	OUT4–A	OUT4–B	OUT5–A
11	OUT5–B	OUT6–A	OUT6–B
12	OUT7–A	OUT7–B	OUT8–A
13	OUT8–B	TX_EN B~	TX_EN A~
14	RESET_IN		CLK/2
15	100 Hz		RESET
16	FTX A	FTX B	F IN
17	D0	D1	D2
18	D3	D4	D5
19	D6	D7	
20	A01	A02	
21	A16		A06
22	A07	A08	A09
23	A10	A11	A12
24	A13	A14	A15
25	S/H IN		
26	XIOW	RESET	XIOR
27	AVEE	AVEE	AVEE
28	AVCC	AVCC	AVCC
29	AGND	AGND	AGND
30			
31	GND	GND	GND
32	VCC	VCC	VCC

P1 Signal descriptions:

IN1–A to IN8–B .... Input channels from transducers
OUT1–A to OUT8–B .... Output to ACM PCB
VCA .... Voltage Control A from IO/M PCB
VCB .... Voltage Control B from IO/M PCB
TX_EN A~ .... Transmit Enable A from CPU
TX_EN B~ .... Transmit Enable B from CPU
RESET IN .... Not used
CLK/2 .... Clock input to PAL from CPU
100 Hz .... Modulation frequency from IO/M
RESET .... From CPU – resets DEMFIL circuit
FTX A .... Transmitter frequency from TxMA
FTX B .... Transmitter frequency from TxMB
F IN .... Bandwidth via U15 to DEMFIL
D0 to D7 .... 8–bit data bus
A01 to A16 .... 16–bit address bus
S/H–IN .... Sample and hold from ADCM
XIOW .... I/O write strobe
XIOR .... I/O read strobe
AVEE .... Analogue –5 Vdc
AVCC .... Analogue +5 Vdc
GND .... Ground
VCC .... Digital +5 Vdc

6.3.5 Maintenance aids

6.3.5.1 Test points

TP 1 .... Transducer signal channel 1, (X)
TP 2 .... Transducer signal channel 2, (Y)
TP 3 .... Transducer signal channel 3, (R)
TP 4 .... Same as channel 3. linked together on input
TP 5 .... Not fitted
TP 6 .... Not fitted
TP 7 .... Not fitted
TP 8 .... Transducer signal channel 8 (Telemetry)

- The demodulator frequency should be present at "Demfil" pins 1 and 2. The frequency should be two times the actual listening frequency. Note that the frequency will shift by the transmitter pulse after the reply is received. (50 Hz off).

- The bandwidth clock should be present on "Demfil" pin 14, and should be 50 times the actual bandwidth.
- The Sample/Hold clock should be present on U13 pin 13, and then go to pin 15 on all the "Demfil" packages.

The signal reply pulses (5 to 7 Vp–p) should be present on the test points in front of the "Demfils". (TPs 1, 2, 3, 4 and 8).

- The signal pulse envelope should be present on "Demfil" pins 27 and 28. Maximum amplitude should be 4 V p–p.

6.3.5.2 Links

- LK1

Link 1–2 . . . . Not used
Link 2–3 . . . . 2 x mod. freq. telemetry normally closed

- LK2

Link 1–2 . . . . Not used
Link 2–3 . . . . Not used

- LK3

Link 1–2 . . . . Not used
Link 2–3 . . . . Not used

- LK4 / LK5

Link 1–2 . . . . Lk 4 pin 2 is linked to Lk 5 pin 2 to set bandwidth for wide and telemetry

6.4 Analogue digital converter (ADCM)

6.4.1 Location and purpose

The Analogue Digital Converter (ADCM) circuit board is located in the third slot from the left. The purpose of the ADCM is to perform analogue to digital conversion. It offers conversion of 32 analogue input channels and temporary storage of data in dual port RAM. Up to eight conversion sequences can be programmed into an EPROM. Data sets are stored alternately in two banks of RAM.

6.4.2 Physical description

The ADCM is designed to the single Euro–card circuit board standard, with four layers. Two layers are used for the signals, two layers are used for the power supply. The board is equipped with two connectors, one located at each end. A 50–pin connector (P2) is the only front mounted device visible when the board is in position in the HPR 400 Transceiver Unit.

6.4.3 Circuit description

The ADCM circuit board provides 32 multiplexed analogue input channels. Dual 16–bit multiplexers are used to select analogue input signals obtained from the sample–and–hold outputs of the Input–M circuit board. Each output from the Input–M provides a real and imaginary analogue signal between ± 2.5 Vdc.

Real and imaginary inputs to the board are connected to two separate multiplexers. The input channels are selected by the multiplexer address lines. An amplifier system is used between each multiplexer and corresponding A/D converter to create a 0 to +5 V input signal range to the A/D from the ± 2.5V signal at the multiplexer input. The 12–bit A/Ds are both controlled by the sequence controller.

The conversions take place simultaneously to provide the shortest possible conversion time for two input signals. However, each A/D is started individually.

The digital outputs from the A/Ds are stored in dual port RAM. A full data set (data from conversion of all 32 input signals) is stored alternately in the two banks to allow the last converted data set to be read from the RAM whilst a new set of conversions is in progress.

Note ! *The maximum time required to convert one data set (all 32 input signals) is 80 µs. This does not include the 4 µs settling time required in sample–and–hold circuits of the DEMFIL devices.*

A 16–bit bi–directional data bus interfaces the ADCM with the other circuit boards.

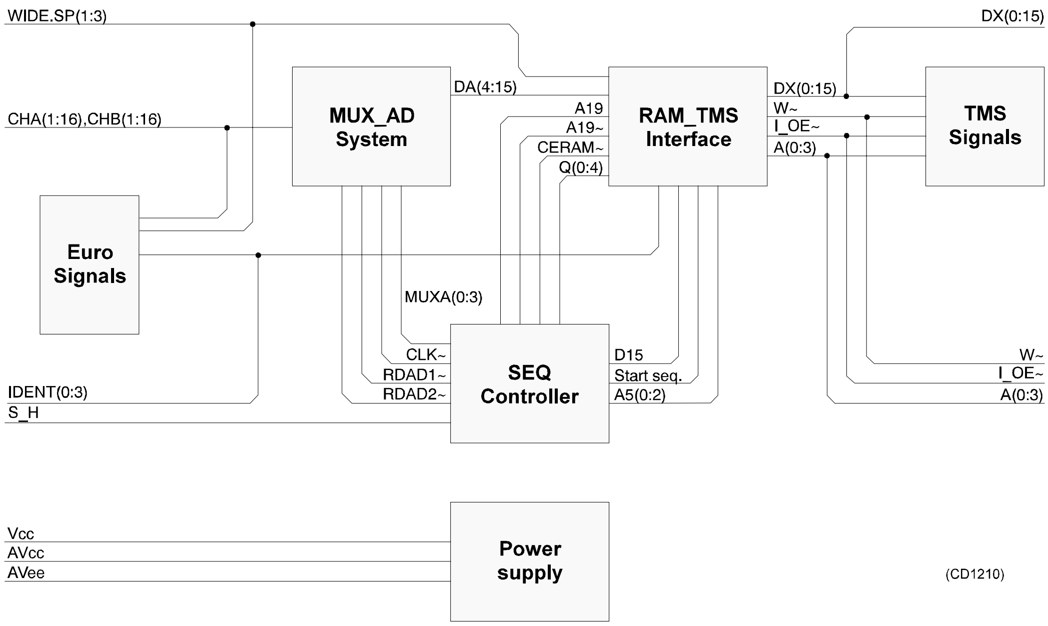

Figure 5 A / D Converter (ADCM) – block diagram

The control lines IDENT(0:3) provide the board with a unique identification code which is set by jumpers S1 – S4. The external address lines A(0:3) must match this code to select the board.

6.4.4 Connections

The board carries two connectors, one located at each end of the board. **P1** is a 96–pin, male, right–angled connector. It connects the ADCM into the motherboard. **P2** is a 50–pin, male, right–angled connector with ejector/latch. It is located on the front edge of the board.

6.4.5 Maintenance aids

6.4.5.1 Test points

TP 1 . . . . ADC, IC4 input (real signal)

TP 2 . . . . ADC, IC4 BUSY~

TP 3 . . . . ADC, IC8 input (imaginary signal)

TP 4 . . . . ADC, IC8 BUSY~

TP 5 . . . . START_SEQ

TP 6 . . . . CLK~

TP 7 . . . . IC21 CK (multiplexer address latch)

TP 8 .... S_H
TP 9 .... +5 Vdc digital
TP 10 .... DGND
TP 11 .... +12 Vdc analogue
TP 12 .... Analogue ground
TP 13 .... –12 Vdc analogue

6.5 Digital signal processor (DSPM 50)

6.5.1 Location and purpose

The Digital Signal Processor (DSPM 50) board is located fourth from the left in the HPR 400 Transceiver Unit rack. It is designed as a general purpose single board computer, and its main task is to perform digital signal processing.

6.5.2 Physical description

The DSPM 50 is a single euro–card circuit board, constructed of eight layers. It holds two LEDs and one 50–pin connector, P2, on its front edge.

6.5.3 Circuit description

The DSPM 50 is a general purpose digital signal processor board. It utilizes the TMS 320C50 Digital Signal Processor manufactured by Texas Instruments. The DSPM 50 operates on a 50 MHz clock frequency, and holds a total of 128 kbyte memory for program and data storage. The program memory is loaded from a main control processor unit (the Central Processing Unit (CPUEX)) through a general bus interface in the 96–pin Europa connector P1.

The processed output from the DSPM 50 is sent through a FIFO (first in / first out) connected to this bus. External input and output signals are connected to the board through the DSPM 50's I/O expansion bus available on the front mounted 50–pin flat ribbon cable connector P2.

The DSPM 50 board comprises the following functional modules:

- Digital Signal Processor
- Memory
- I/O Expansion Bus
- FIFO Buffer
- 11 Digital Inputs
- 16 Digital Outputs
- Control circuitry
- Bus Interface
- Power +5 Vdc (250 mA typical)

The Texas Instrument signal processor is a fixed point 16–bit processor with a 16–bit address bus. The DSPM 50 has separate program and data addressing space.

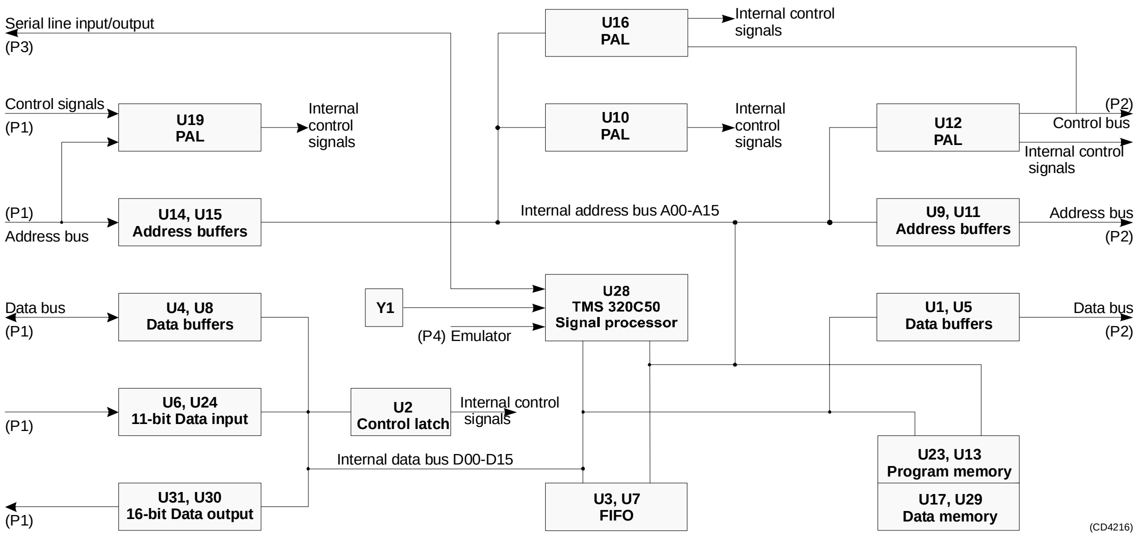

Figure 6 Digital Signal Processor (DSPM 50) – block diagram

U13 and U23 are the program memory units, and U17 and U29 are the data memory. Both memories can be read or written to from an external computer.

The signals from the TMS320C50 and the PAL U10 supply all the control signals to the memories. U10 also controls the memory when a external computer is controlling the board, and the external computer can take control of the address bus by buffers U14 and U15. U4 and U8 are the data buffers transceivers. U19 decodes the external computer address bus and read write signals, and generates control signals (SEL1, SEL2, MWR/ and MRD/) to U10 to control the memory. U19 also supplies the latch signal to the control latch U2, and the read signal to the FIFO's U3 and U7. U19 also controls the enabling of the bus buffers and the direction of the data buffer transceivers.

The control latch U2 is written to by the external computer. DB00 controls the HOLD/ signal of the DSPM 50, and floats the DSPM 50 before an external computer takes control of the board's internal bus. DB01 is used for resetting the DSPM 50 after a new program is loaded into the program memory from an external computer. DB07 resets the output FIFO buffer.

Y1 is a crystal oscillator supplying the frequency needed by the DSP.

Serial line signals CLKR, CLKX, DR, DX, TCLKR, TCLKX, TDR, TFSR, TFSX, TDX, FSR and FSX are connected directly from the DSP to P3.

The board requires +5 Vdc, and consumes approximately 250 mA.

6.5.4 Connections

The MUNAV Digital Signal Processor (DSPM 50) holds two connectors (with place for two more which are not used in the HPR 400 system):

P1 .... 96–pin, male, right–angled Europa connector placed at the back edge of the circuit board

P2 ...... 50–pin, male, low–profile flat ribbon cable connector placed at the front edge of the circuit board

P3 .... Serial line connector – not used

P4 .... Emulator connector – not used

6.5.5 Maintenance aids

6.5.5.1 Test points

TP1 .... FIFO Empty flag

The user may check basic functions by using an oscilloscope and measure on the following points:

- The HOLD/ signal on U2 pin–2 and RS/ on U2 pin–5. These must both be low when loading the program memory.
- The signal STRB/ on U16 pin–4. A pulse train will be observed when the signal processor is running.

6.5.5.2 Links

Lk 1 .... Normally on – enables D1

Lk 2 .... Normally on – connects HOLD/ to TMS320C50

Lk 3 .... Normally on – enables D2

Lk 4 .... Normally on – connects RS/ from U2

Lk 5 .... Normally open – selects clock option

Lk 6 .... Normally open – selects clock option

Lk 7 Used for test, Normally on – connects clock to TMS320C50

Lk 8 . . Normally open – selects MP or MC mode of TMS320C50

Lk 9 .... GND

Lk 10 .... +5 V

Lk 11 .... Normally A. A selects A14, B selects A15 to program ram P3

6.5.5.3 LEDs

LED D1 .... On when FIFO is empty

LED D2 .... On when board is running

6.6 Transmitter (TXM)

6.6.1 Purpose

Two Transmitter (TXM) boards are used in the HPR 400 Transceiver Unit. These are TXM–A and TXM–B. The Transmitter board (TXM) is a general purpose transmitter, containing its own frequency generator, power control and power supply circuits (the board feeds both the Rx and CPU circuit boards when in the Mutran mode). The two boards used in the system are identical in all respects.

6.6.2 Board description

The TXM is designed to the single Euro–card standard, and comprises four layers.

6.6.3 Front mounted devices

The TXM board holds two test points and two factory–set links on its front edge.

6.6.4 Circuit description

The transmitter board holds two MAX663 voltage regulators which provide the voltages used in the transmitter. It also has a crystal oscillator which is used as the Tx frequency source and a direct numerical synthesizer for generating the correct Tx frequency. Driver stages with power control, an output stage with over–current protection, transducer matching circuits and a transducer relay complete the board.

The crystal oscillator runs at 3.2768 MHZ, and is switched on and off by the MCU (TXOSC). The oscillator frequency is fed to a counter chain via latches. The counter chain is also loaded with a 2 x 8 bit word from the MCU, determining the division factor in the chain. This method of generating transmitter frequencies makes it possible to alter the frequency instantaneously, a necessary feature in telemetry applications.

The output from the counter chain, called S8, is combined with the TX–EN signal and forms the tone–burst, normally 10 ms, to feed the driver and output stages.

The transistors in the output stage are switched on for varying fractions of the half–period of the output signal. Thus the area of each half–period can be varied to control the output power without varying the supply voltage to the output stage. As the half–periods are narrowed the energy contained in the signal is reduced, and after being shaped in the output transformer and the transducer matching circuits, the amplitude of the signal driving the transducer elements will be lower.

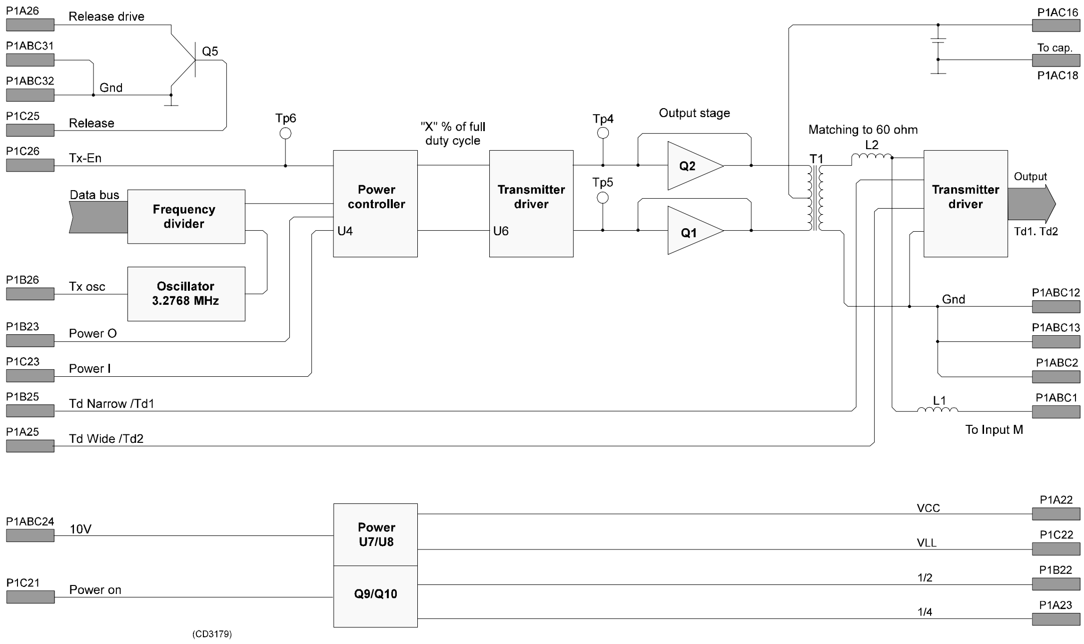

Figure 7 The Transmitter circuit board – block diagram

The driver signals are fed to the output transistors via two paths which are 180 out of phase. This is because the output stage is a push–pull circuit where transistors Q1 and Q2 alternately pump current through transformer T1 for one half–period each.

The output from the transistor stage is fed through a relay, providing the possibility to choose between different transducer elements for beam selection. The relay is a bistable relay, i.e. it is stable in both positions and therefore does not consume any power in either position. The relay is operated by sending a current pulse through one of the internal coils. The beam switch control signals are generated by the micro–controller board.

The transmitter board also contains a release driver stage. Transistor Q5 acts a power switch for the release motor, controlled by the micro–controller.

6.6.5 Socket–mounted components

U5 (PAL) .... Programmable I/O controller

6.6.6 Connections

The board has one 96–pin, male, right–angled connector (P1) located on the rear edge of the board to link the board into the backplane.

6.6.7 Maintenance aids

6.6.7.1 Oscilloscope test points

The following oscilloscope test points are available to assist the maintenance engineer:

TP1 . . . . FTx, 50% duty cycle

TP2 . . . . Transmitter pulse, 10 ms, voltage depending on power

TP3 . . . . +10 V when POWERON is ON, (**Mutran**).
+15 V for **Munav**

TP4 . . . . 10 ms burst to Tx driver, duty cycle dep. on power control. +5 V when POWERON is ON

TP5 . . . . 180 out of phase with TP4"

TP6 . . . . +5 V, 10 ms pulse from CPUM

TP7 . . . . GND

6.6.7.2 Links

The TXM board holds the following links:

LK1 . . . . Link 1–2 if U5(Pal) is in use. Normally closed
Link 2–3 for external frequency burst

LK2 . . . . Link 1–2 if U5(Pal) is in use. Normally closed
Link 2–3 for external frequency burst

LK3 . . . . Closed

LK3 . . . . Depending on application

LK4 . . . . Closed

LK4 . . . . Depending on application

LK5 . . . . Closed

LK5 . . . . Depending on application

LK6 . . . . Closed

LK6 . . . . Depending on application

LK7 . . . . Closed

LK7 . . . . Depending on application

6.6.7.3 Switches

The TXM board holds no switches.

6.7 "Powerbox" AC power supply

6.7.1 Purpose

The **POWERBOX ESA–K105U/XS** AC power supply enables the HPR 400 system to be powered from a 230 Vac supply.

6.7.2 Board description

The unit is purchased from an external supplier. It is based on a commercially available power supply, though has been altered to Simrad's specifications. The unit is open to allow cooling air around the componants, but is designated "Repair by replacement". It is designed to be installed in a standard 19 rack.

6.7.3 Technical specifications

The unit physical specifications are as follows:

Width . . . . 12 TE

Height . . . . 111 mm

Length . . . . 168.5 mm

Weight . . . . 700 g

Operating temperature . . . . 0°C to 80°C

Storage temperature . . . . –25°C to +85°C

Efficiency . . . . 80% typical

Isolation and safety . . . . To EN 60 950

EMI/RFI standards . . . . To EN 55 022B (VDE 0871 B)

6.7.4 Electrical characteristics

The unit requires a supply of 230 Vac or 115 Vac[1], and provides an output of 48 Vdc, 2 A (4 A peak).

6.7.5 Socket–mounted components

None – this power supply is a sealed unit and must not be "adjusted" by the system maintainer.

1 Switching between 115 Vac and 230 Vac is performed using straps inside the unit.

6.7.6 Connections

The power supply unit is plugged into the backplane by a connector comprising fifteen 5 mm spade terminals. The terminals are allocated as follows:

P1 pin allocation 15-pin connection block	
Pin	**Signal description**
4	+ Vo1
6	+ Vo1
8	+ Vo1
10	+ S
12	– S
14	– Vo1
16	– Vo1
18	– Vo1
20	
22	
24	
26	
28	230 Vac in (L)
30	230 Vac in (N)
32	GND

6.7.7 Maintenance aids

This power supply is a sealed unit. In the event of malfunction, replace the unit.

6.7.8 LEDs

The front of the unit holds 1 green LED which indicates the existence of the 48 Vdc output.

6.7.9 Fuses

The unit holds an input fuse, located in the rear of the unit, to protect it in the event of severe defects. The fuse is:

- 5 mm x 20 mm, 250 V, 2.5 A, slow-blow

Caution ! *Nothing else must be used.*

6.8 Control processing unit (CPUEX)

6.8.1 Location and purpose

The Control Processor Unit (CPUEX) is the fifth board from the left in the rack. The CPUEX is a single–board computer utilizing the 80386EX microprocessor. The purpose of the board is to control the operation of the HPR 400 Transceiver Unit.

6.8.2 Physical description

The CPUEX is a standard eight–layer single–Europe board. One edge connector connects to the motherboard. The front edge holds a 34–pin connector, four LEDs, two test points and link Lk7.

6.8.3 Circuit description

The CPUEX is designed as a Control Processor Unit using the 80386EX microprocessor from Intel. The board has sockets for an 80387SL numeric processor and flash memory. The board also holds RAM memory for program and data storage, serial lines, interrupt inputs, general I/O lines and a general bus interface (96–pin Europa connector).

The 80386EX CPU is the main controller on the circuit board. It is a 16–bit microprocessor, working internally with 32–bits, and it is software compatible with 80386 software used on normal personal computers. Addressing capability is up to 16 Mb. A 32 MHz crystal oscillator supplies the frequency making the 16 MHz CPU clock. A numeric coprocessor 80387SL is mounted.

Two 32–pin PLCC sockets support the flash memory part of the circuit, U6 and U7. These devices are 8–bit wide memory devices. The RAM memory consists of U8 and U9. One is for the 8–bit low byte and one for the 8–bit high byte.

The Bus Interface contains address buffers and bidirectional data buffers to the system bus, which is in the 96–pin Europa connector.

The board contains 6 TTL inputs (ID1 to ID6), 12 TTL outputs (ID9 to ID16 and OUT1 to OUT4), nine external interrupt inputs and six 16–bit timers.

Two separate serial lines with separate programmable baud–rate control are available. Selection between RS 232 and RS 422 is made by links on the inputs. Both serial lines supply RS 232 and RS 422 as outputs at the same time.

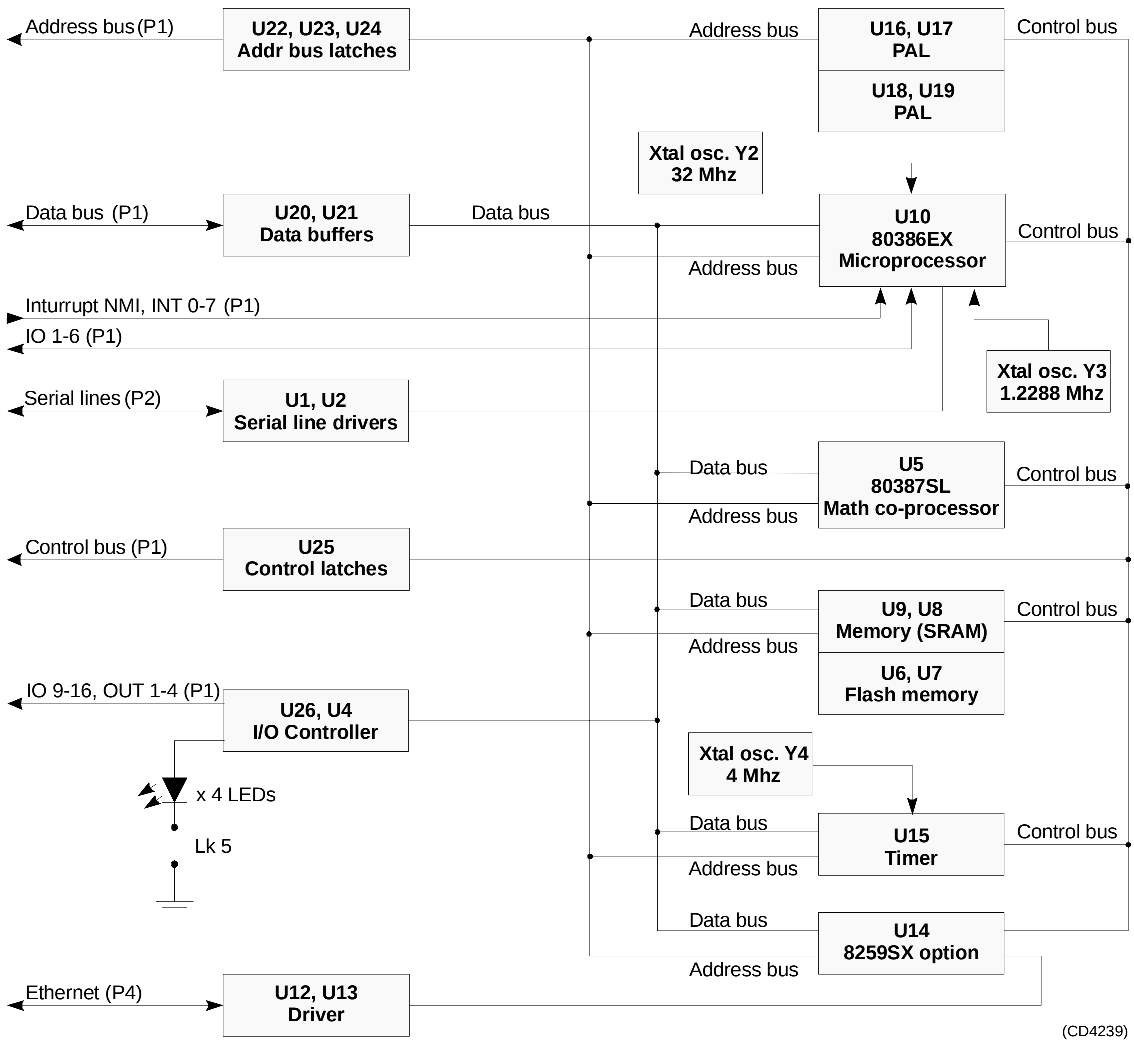

Figure 8 Control processor unit (CPUEX) circuit board – block diagram

6.8.4 Connections

There are two connectors; one placed at each end of the circuit board.

P1 . . . . 96–pin, male, right–angled Europa connector

P2 . . . . 34–pin, male, flat ribbon cable connector

6.8.5 Maintenance aids

6.8.5.1 Test points

TP 1 . . . . GND

TP 2 . . . . +5 V

6.8.5.2 Links

LK 01 .... Link 1–2 for RS 422 input serial line A
Link 2–3 for RS 232 input serial line A

LK 02 .... Link 1–2 for RS 422 input serial line B
Link 2–3 for RS 232 input serial line B

LK 03 .... Normally closed, software control

LK 04 .... Ram dependent

LK 05 .... On = enables D1 – D4

LK 06 .... On = WD enable

LK 07 .... Reset connector

6.8.5.3 LEDs

D1 –D4 .... Software–controlled, front mounted

6.8.5.4 Oscilloscope check points

The maintenance engineer can check the basic functions by using an oscilloscope and measuring on the following points:

- The signal ADS/ on U16 Pin 3, observe the pulses when the board is (should be) running. Check for one positive pulse to start every instruction cycle.

6.9 Input/output board (IO/M)

6.9.1 Purpose

The Input/Output board (IO/M) is designed to the single Euro–card circuit board standard. It is designed to interface the most common HPR SSBL and LBL inputs and outputs, such as a vertical reference unit, course gyro, external synchronization and serial lines.

6.9.2 Board description

The vertical reference unit, gyro and serial line 1 (to the system controller) are galvanically isolated. Serial lines 2 and 3 are dedicated to tracking interface. These serial lines are galvanically isolated on the Serial Interface board, SIF.

Serial line 1 is available with a programmable baud–rate control, coming from the CPU board. Selection between RS232 and RS422 is made using links on the inputs. The serial line may also be inverted by links on the board. The serial line may supply RS232 and RS422 as outputs simultaneously.

Serial lines 2 and 3 are RS422 only, controlled by U3, 82530.

6.9.3 Front mounted devices

A 50–pin connector, P2, is the only device mounted on the front edge of the board.

6.9.4 Circuit description

All decoding is implemented with PALs, and may thus be reconfigured. The PAL 22V10 (U11) is the main decoder in the system. It initiates Chip Select to all the different devices and functions, and also generates RD (read) and WR (write) strobes to the 82530.

U13 is the address buffer for the system bus. It contains two address bits. The bus is available on P1. U5 and U6 are the bidirectional data transceivers. The data bus is also available on P1.

The 82530 (U3) Serial Communication Controller contains two serial lines identified as 2 and 3".

Four analogue inputs are supported, made switchable by means of the U10 multiplexer. Two of the inputs are dedicated for Roll and Pitch inputs from an external vertical reference unit (VRU).

Four analogue outputs are provided. These are originally designated as TVG outputs (Time Varied Gain) to preamplifier boards and/or transducers. The analogue outputs are generated by the D/A converter U20.

One synchro input intended for a course gyro input, and two differential inputs, are provided.

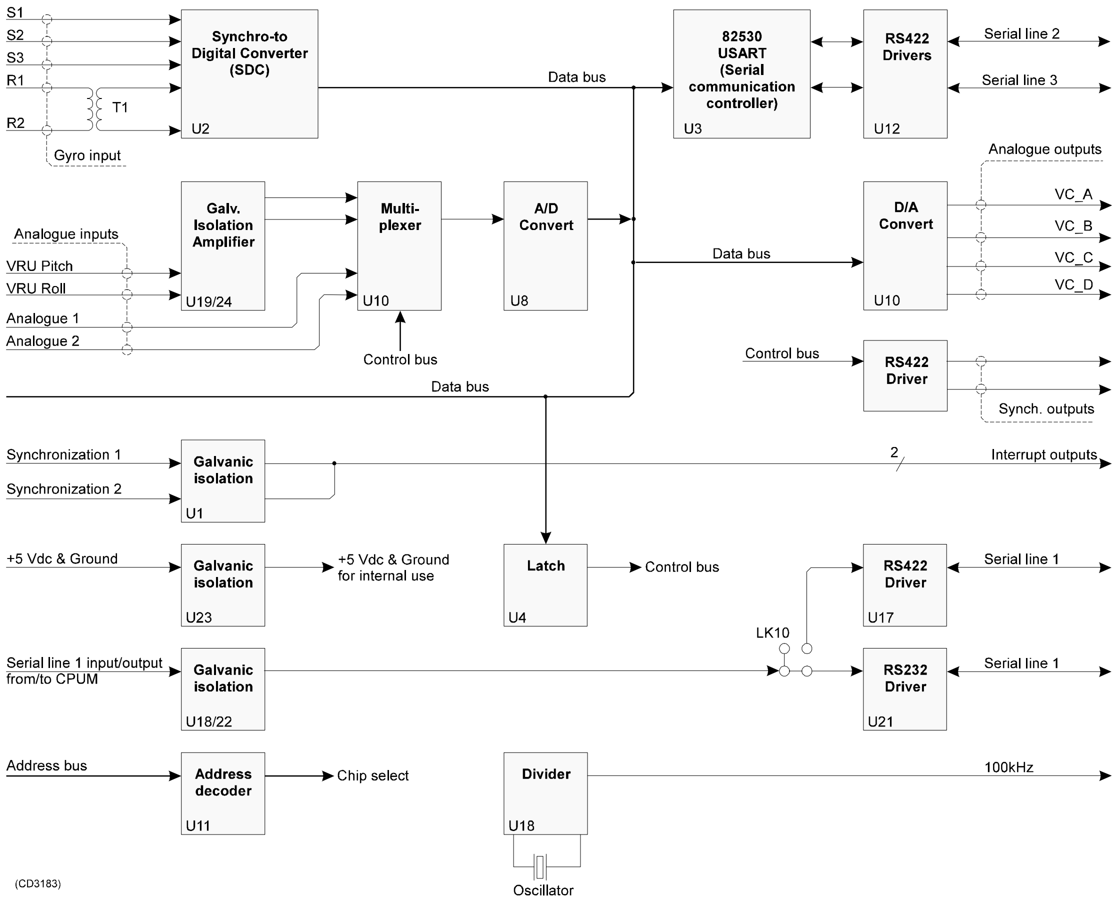

Figure 9 The Input/Output circuit board (I/OM) – block diagram

6.9.5 Socket–mounted components

U 02 . . . . Synchro to digital converter SDC–19204–302. 26 Vac 50/60 Hz

U 03 . . . . Intel P82530–6 Serial communication controller

U 11 . . . . PAL 22V10 address decoder

U 12 . . . . DS 8922 RS422 Driver/Receiver

U 17 . . . . DS 8922 RS422 Driver/Receiver

U 21 . . . . MAX233 RS232 Driver/Receiver

6.9.6 Connections

There are two connectors; one at each end of the circuit board.

P1 . . . . 96–pin, male, right–angled connector

P2 . . . . 50–pin, male, flat ribbon cable connector

6.9.7 Maintenance aids

6.9.7.1 Test points

TP 01 .... GND
TP 02 .... Analogue inputs, between multiplexer and AD
TP 03 .... Pitch
TP 04 .... Roll
TP 05 VCC
TP 06 .... VCC1
TP 07 .... GND1
TP 08 .... Pitch input
TP 09 .... VRU common
TP 10 .... Roll input

6.9.7.2 Links

LK 01 .... Link 1–2 for direct Analog_1 input
Link 2–3 for Analog_1 input via amplifier.

LK 02 .... Link 1–2 for direct Analog_2 input
Link 2–3 for Analog_2 input via amplifier.

LK 03 .... Link between analogue and digital ground
Normally closed.

LK 04 ..... Digital ground to D/A converter. Normally closed.

LK 05 .... –5 Vdc to D/A converter.

LK 06 .... A/D converter 20 V input. Normally closed.

LK 07 .... A/D converter 10 V input.

LK 08 .... Link 1–2 for inverted Serial line 1, Tx.
Link 2–3 for non–inverted Serial line 1, Tx.
Normally closed.

LK 09 .... Link 1–2 for inverted Serial line 1, Rx.
Link 2–3 for non–inverted Serial line 1, Rx.
Normally closed.

LK 10 .... Link 1–2 for RS422 input serial line 1
Normally closed.
Link 2–3 for RS232 input serial line 1.

LK 11 .... Analogue ground to D/A converter.

LK 12 .... 200 Hz reference frequency

LK 13 .... 100 Hz reference frequency. Normally closed.

6.9.7.3 Potentiometers

R 13 .... Adjustment of bipolar offset, A/D converter.
R 14 .... Adjustment of reference voltage A/D converter.

6.9.7.4 Switches

The IO/M board holds no switches.

6.10 The responder controller (RPC) board

6.10.1 Purpose

The purpose of the responder controller (RPC) board is to provide responder trigger pulses as ordered by the HPR system.

6.10.2 Board description

The RPC is designed to the single Euro–card standard. The board holds four identical opto–isolated responder trigger circuits, and communicates with the TMC board in the PC via a flat cable.

6.10.3 Front mounted devices

The RPC board carries four fuses and a diode mounted on its front edge.

6.10.4 Circuit description

Component U10 is the board's data buffer, and component U9 is its control buffer. Card selection is performed by U4, U7, U2 and U3. The card selector output goes high when the RPC has been selected, and flashes the LED D2. U12 is a test latch used to check the RPC board performance.

The RPC board's address is set by means of the DIL switch U2.

Pin 12 of U11 goes low whenever the direct address instruction is executed, causing the bit pattern on the data bus to be latched into U15. The code latched in U15 determines which of the trigger circuits is to be activated. When the trigger instruction is executed, the one–shot U14 applies a pulse of approximately 5.5 ms to pin 1 of U15. The outputs of U15 that are active will draw current through the associated opto–coupler, which again causes a trigger pulse to be generated.

Each trigger pulse circuit is protected by a fuse which also secures the supply voltage to the responder. The trigger pulses are brought out between terminals A / C28 and A8, A10, A12 and A14.

6.10.5 Socket–mounted components

The board carries no socket–mounted components.

6.10.6 Connections

The board holds one connector, P1, located on the back edge of the board. This connects the board into the Transceiver Unit backplane.

P1 .... 64–pin, male, right–angled connector

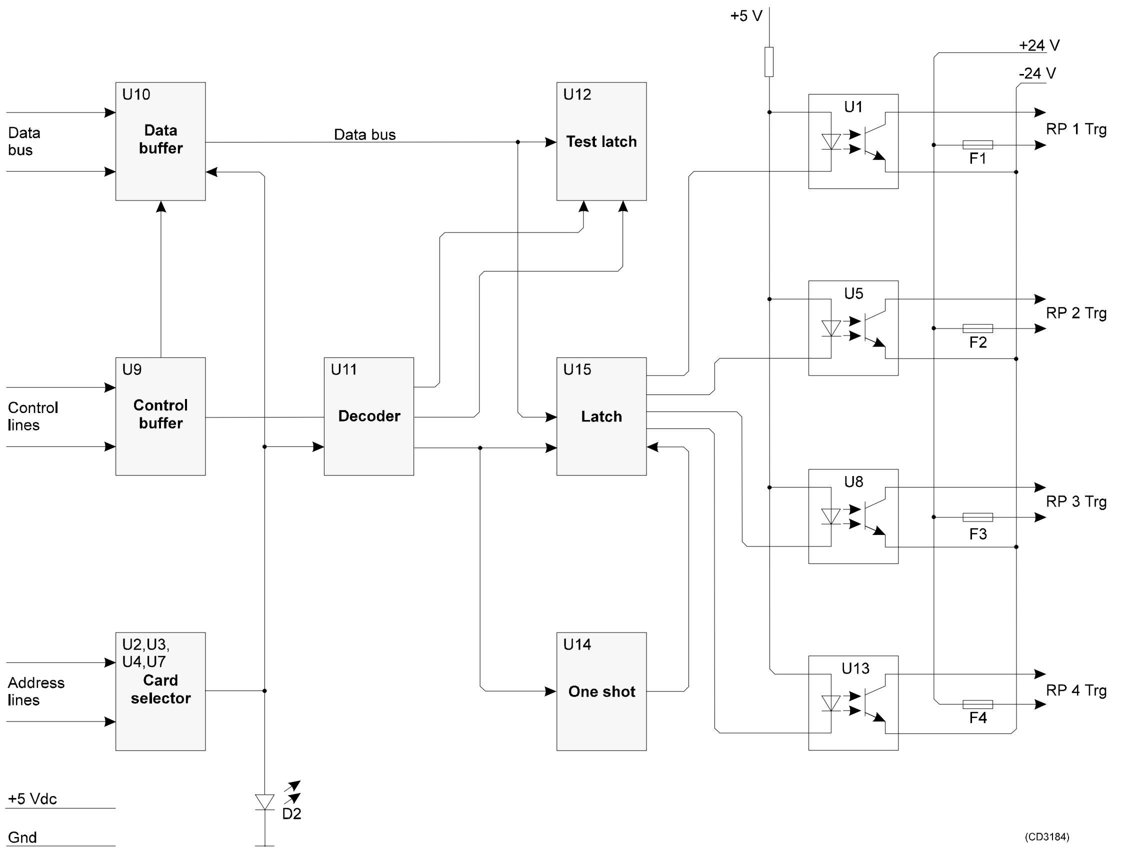

Figure 10 The Responder Controller circuit board – block diagram

6.10.7 Maintenance aids

6.10.7.1 Test points and links

LK1 . . . . Connected only when 24 V is supplied and U16 is not mounted

LK2 . . . . Always connected

6.10.7.2 Switches

Dil switch U2 . . . . Address switch block

Switches 1, 2 and 3 must be set to ON, switches 4, 5, 6, 7 and 8 must be set to OFF.

6.10.7.3 LEDS

D2 . . . . Lights when board is transmitting

6.10.7.4 Fuses

The board carries four 0.1 A, slow–blow fuses, on the +24 Vdc lines.

6.11 DC power supply (DC – PWR)

The DC–PWR is located second from the right in the rack. The board is designed by Simrad, though the power converter units mounted on the board are bought from an external source.

6.11.1 Purpose

The purpose of the MUNAV Power Supply (POWERM) is to supply the electronic circuitry with low level DC voltages. The unit can provide several different voltages, in this system 15 Vdc is used.

6.11.2 Board description

This DC supply is based on EriPower DC–DC converters, which produce the following voltages:

- +5 Vdc
- +15 Vdc
- –15 Vdc

The ±15 Vdc is converted to ±5 Vdc by means of serial regulators.

Two converters are used, one mounted directly onto the board, the other mounted piggy–back fashion on the solder side of the board. The front of the board comprises a black aluminium heat sink. The 48 Vdc input power to the board can be supplied to two different input lines: DC–IN1 and DC–IN2. The board also holds a 2 A constant current output.

6.11.3 Circuit description

When a TTL level signal is applied to either POWER–ON or POWER–UP, the gate on Q1 will be forced to a low level by Q2. This will set the Q2 to a ON condition, and thus pass this power, supplied to input DC–IN1 or DC–IN2.

Note ! *There is a start–up delay of approximately 40 ms between the arrival of a Power On pulse and a settled +5 Vdc output.*

The constant current block is based on a three–terminal voltage regulator (U1) LM317HVK and a serial resistor (R1). The output current will increase until the voltage across R1 is equal to V_{REF}. (1.2 Vdc). A 1 Ω resistor gives a current of approximately 1.2 A.

The DC–DC converter used is a 25W EriPower PKA4000 series, requiring an input voltage between 39 Vdc and 64 Vdc.

The output data is as follows:

+5 Vdc output:

Nominal load . . . . 3.1 A

Maximum load . . . . 5 A

±15 Vdc output:

Nominal load . . . . 0.31 A

Maximum load . . . . 0.8 A

WARNING ! The total load must never exceed 25 W for each EriPower unit, i.e. 50 W in total.

To generate the ±5 Vdc analogue voltage (AVCC/AVEE) the ±15 Vdc outputs from the DC–DC converter are fed to U2 and U3.

6.11.4 Socket–mounted components

The board holds no socket mounted components.

6.11.5 Connections

The board carries one 96–pin Europa connector to link it into the Transceiver Unit's backplane.

P1 pin assignment 96-pin Europa connector			
Pin	**A**	**B**	**C**
1	VCC	VCC	VCC
2	GND	GND	GND
3			
4	DC–IN1	DC–IN1	DC–IN1
5	DC–IN1	DC–IN1	DC–IN1
6	GND	GND	GND
7	GND	GND	GND
8	DC–IN2	DC–IN2	DC–IN2
9	DC–IN2	DC–IN2	DC–IN2
10	GND	GND	GND
11	GND		GND
12	U–STBY	GND	U–STBY
13		U–STBY	
14	CAP–POS		CAP–POS
15		CAP–POS	
16	GND		GND
17		GND	
18	POWER–ON		POWER–ON
19			
20			BATT
21			
22			
23			
24	AVCC (+5 Vdc)	AVCC (+5 Vdc)	AVCC (+5 Vdc)
25	GND	GND	GND
26	AVEE (–5 Vdc)	AVEE (–5 Vdc)	AVEE (–5 Vdc)
27			
28	AVFF (–15 Vdc)	AVFF (–15 Vdc)	AVFF (–15 Vdc)
29	GND	GND	GND
30	AVBB (+15 Vdc)	AVBB (+15 Vdc)	AVBB (+15 Vdc)
31	GND	GND	GND
32	VCC	VCC	VCC

Signal descriptions, inputs:

DC–IN1 . . . . Main DC power source to the board

DC–IN2 . . . . Backup DC power source to the board

Power–ON . . . . Switches power ON (1) or OFF (0) TTL level signal

Power–UP . . . . Switches power ON (1) or OFF (0) TTL level signal

Signal descriptions, outputs:

VCC . . . . +5 Vdc, digital power max. 4 A (8 A)

AVBB . . . . +15 Vdc power max 0.7 A (1.4 A)

AVFF . . . . –15 Vdc power max 0.7 A (1.4 A)

AVCC . . . . +5 Vdc analogue power max 0.7 A (1.4 A)

AVEE . . . . –5 Vdc analogue power max 0.7 A (1.4 A)

U–STBY . . . . Unswitched supply, outputs the highest input voltage – 1 Vdc

CAP–POS . . . . Transmitter supply, constant charge circuit of 1.2 A

BATT . . . . This output gives a high level when the main DC power source voltage drops below the backup DC power source voltage

6.11.6 Maintenance aids

6.11.6.1 Test points

TP1 . . . . + 5 V digital

TP2 . . . . Digital ground

TP3 . . . . + 48 V analogue input

TP4 . . . . Analogue ground input

TP5 . . . . Analogue ground output

TP6 . . . . – 15 V analogue output

TP7 . . . . + 5 V analogue output

TP8 . . . . + 15 V analogue output

6.11.6.2 Links

The board has a link field (LKI) comprising four links S1, S2, S3 and S4. These links are used to swap polarity on the DC–DC converted input pins.

A 48 volt supply requires S1 and S3 to be closed.

6.11.6.3 Switches

The board holds no switches.

7 REPLACEMENT OF PARTS

7.1 General

The following circuit boards contained in the Transceiver Unit are defined as Line Replaceable Units (LRUs):

- The backplane.
- Input M – A/B.
- A/D Converter (ACM).
- Digital Signal Processor (DSPM).
- Control Processing Unit (CPU).
- Ethernet.
- Input/Output (IOM).
- Responder (RPC).
- Transmitter (TxM – A/B).
- DC Power supply (DC – PWR).
- AC Power supply (AC – PWR).

The removal and replacement of these parts is described in the following paragraphs.

Note ! *The maintenance engineer must wear a grounding bracelet which is securely connected to the vessel's ground at all times when performing maintenance on the Transceiver Unit.*

7.2 Replacement of circuit boards and software

The circuit boards in the Transceiver Unit are all plug–in modules which are easily replaceable. A special extraction tool (wire hooks) will considerably simplify the removal operation, and a small screw–driver may be required to open the front panel. All the boards and power units are replaced using the same procedure.

7.2.1 Removal of circuit boards

Removal of a board is performed according to the following procedure:

Note ! *If the Transceiver Unit is installed in a console or a rack, the operation may be simplified by removing the unit to a work–bench before proceeding with the circuit board replacement.*

1 Ensure all power to the HPR system, and to other systems connected to the HPR system (e.g. DPS, vertical reference unit etc.) is switched off. Remove the system fuses if possible, and label the fuse panel with a tag stating that maintenance is being carried out on the system.

2 Using a small screw–driver if necessary, open the Transceiver Unit front panel. This is achieved by slackening the two captive screws in the upper corners and hinging the panel downwards. The panel must be allowed to swing below the horizontal if circuit boards are to be removed, so the unit may need to be supported on blocks.

3 Locate the desired circuit board and carefully remove any connectors which may be attached to the front of the board. This will not be easy.

4 Locate the extraction tool hooks into the holes in the upper and lower corners of the board's front edge and carefully pull the circuit board straight out from the Transceiver Unit rack.

Note ! *Most of the circuit boards hold software in EPROMS, PROMs and PALs. If a board is to be replaced, the software will have to be moved over to the new board. Also, several links and switches must be set correctly to ensure proper operation. When replacing a circuit board, ensure that the new links and switches match the old .*

7.2.2 Software replacement

Replacing the software, or moving it to a new board, is a delicate job and must be handled with extreme care. The following precautions must be taken:

1 The replacement operation must be performed on a clean and stable workbench or table.

2 The table must be covered with an anti–static mat connected to the ship's ground.

3 The maintenance engineer MUST wear a grounding bracelet connected to the ship's ground.

4 Each software device is identified with a white label. This label holds the following information:

– Circuit board	E.g. DSPM
– Device number	E.g. U15
– Software version	E.g. V1.1
– Date	E.g. 92.09.15
– Check sum (in hexadecimal)	E.g. 05A3

7.2.2.1 Removal

1 Identify the device to be removed, and write down the location of pin.1.

2 Using a small screwdriver or a special extraction tool, remove the device carefully from its socket on the source circuit board. Ensure the device is lifted as vertically as possible to prevent damage to the pins. Once removed, handle the device with care.

7.2.2.2 Insertion

Identify the socket where the device is to be located.

Place the device carefully into the socket, and ensure it is orientated correctly.

Check that all the pins are in the correct holes in the socket, then press the device firmly and evenly into the socket.

After insertion, check that all the pins are properly inserted into the socket and that no pins are bent.

7.2.3 Removal of the backplane

The backplane is located behind the circuit boards, and is accessible through the back of the unit. All the circuit boards and power units must be removed through the front of the unit before the backplane can be removed. All connections to the backplane are made using plugs.

Remove the backplane following the procedure below:

Note ! *If the Transceiver Unit is installed in a console or a rack, the unit will need to be extracted and taken to a work–bench before proceeding with the backplane removal procedure.*

1 Ensure all power to the HPR system, and to other systems connected to the HPR system (e.g. DPS, vertical reference unit etc.) is switched off. Remove the system fuses if possible, and label the fuse panel with a tag stating that maintenance is being carried out on the system.

2 Label all the cables connected into the back of the Transceiver Unit, and disconnect them.

3 Remove all the circuit boards and power units using the procedure given in paragraph . Ensure the boards are placed in a safe place.

4 Using a small screw–driver, remove the 12 screws securing the Transceiver Unit rear panel in position. The panel is now attached to the unit only by the cables.

5 Using a suitable insulated tool or wire link, discharge the two large capacitors located towards the left side of the rear panel.

6 Remove all the connecters attached to the backplane. The backplane should now be readily accessible.

7 Slacken and remove the 18 screws securing the backplane into the Transceiver Unit. The backplane should now be loose, and the engineer can remove it carefully through the back of the unit.

If the backplane is going to be out of the Transceiver Unit for some time, it is recommended to replace the circuit boards into the front of the unit and close the unit to protect the boards.

7.2.4 Replacement of the backplane

Replacing the backplane is a reversal of the procedure given in paragraph

Care should be exercised to ensure that parts fit together correctly before securing screws are tightened. Do not attempt to apply force to any of the parts. Do not over tighten the securing screws.

7.2.5 Replacement of circuit boards

When replacing a board into the rack, care must be exercised to ensure that the board is correctly positioned in the rails before any pressure is applied to the board. If the rear mounted connector pins are damaged, a replacement board will be required.

1 Ensure all power to the HPR system, and to other systems connected to the HPR system (e.g. DPS, vertical reference unit etc.) is switched off. Remove the system fuses if possible, and label the fuse panel with a tag stating that maintenance is being carried out on the system.

2 Locate the correct slot for the board in question. Note that the slots are identified by the board's initials, and the boards are identified by text written onto the component side. In all cases, the board must be located such that the components are to the right of the board.

3 Locate the board in the slots and carefully slide the board into the unit. Ensure that the board does not interfere with and cables as it is pushed in. If necessary, hold any cables which may be obstructing the board out from the unit.

4 When the connectors on the back of the board begin to mate with the connectors on the back plane, (approximately 5 mm before the board is fully home) check that the board is correctly located then apply even pressure over the front of the board and push it firmly home.

5 When the front of the board is fully home, the black plastic board retention clip will latch over the upper edge of the board to keep it in position.

6 Carefully replace the front connector (if applicable), ensuring it is pressed fully into the socket.

7 Once all the boards are in position, close the front of the Transceiver Unit. Ensure that the power cable towards the right side of the unit is not crimped as the panel is closed. Secure the panel closed using the two screws in the upper corners.

7.3 Replacement of fuses

7.3.1 Fuse locations

The Transceiver Unit has two mains input fuses, held in fuse holders located towards the left side of the rear panel (when seen from the rear). A further four fuses are located on the Responder board (though as this board is optional it may not be included in the Transceiver Unit), and the AC power supply holds one.

The fuses are as follows:

- On the rear panel
  - For 115/230 Vac supply – 5 mm x 30 mm, 2 A, slow–blow.
  - For 115/230 Vac supply – 5 mm x 30 mm, 2 A, slow–blow.
- On the Responder board

  Four fuse holders are mounted on the board. The fuses to be used are

  - 5 mm x 20 mm, 0.1 A, 24 Vdc, slow–blow.
- In the AC power supply

  The fuse is contained in a holder located on the rear of the unit. The fuse to be used is:

  - 5 mm x 20 mm, 250 V, 2.5 A, slow–blow.

Caution ! ***Never attempt to use any other size of fuses than those stated.***

7.3.2 Fuse replacement

1 Switch off the entire HPR system, including other external units which are connected to the HPR system.

2 If the suspect fuse is located on a circuit board, remove the board from the Transceiver Unit following the procedure described in paragraph . Replace the blown fuse(s) with the correct size and type of fuse.

Caution ! ***NEVER attempt to use anything except the correct size and type of fuse in the fuse holders. Irreparable damage may be caused to the Transceiver Unit if the wrong fuses (or anything else) are used.***

3 Return power to the HPR system, then to the other external units.

Note ! *If, when a fuse is replaced, it blows again when power is switched on to the system, a more serious fault exists. Do not replace the fuses a second time till the fault has been located and corrected.*

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